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INFORMATION CITED BY APPLICANT(S) THAT MAY BE MATERIAL TO THE PROSECUTION OF THE SUBJECT APPLICATION

Applicant: Jee-Soo Mok, Byung-Kook Sun,
Chang-Kyu Song, Geum-Hee Yun,
Tae-Hoon Kim

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Application No.: 10/717977
(filed concurrently)

Group Art Unit: 282~

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Examiner:

Title: PARALLEL MULTI-LAYER PRINTED CIRCUIT BOARD HAVING IMPROVED
INTERCONNECTION AND METHOD FOR MANUFACTURING THE SAME

U.S. PATENT DOCUMENTS

*Examiner Cite	Kind	Date	
Initials No. Document No.	Code	(mm/dd/yyyy)	Name
None			

FOREIGN PATENT DOCUMENTS

*Examiner Cite	Kind	Publication Date		English
Initial No. Document No.	Code	(mm/dd/yyyy)	Country	Abstract Translation Provided Provided
<u>mt</u> F1 WO 01/39267	A1	5/31/2001	Japan	X No

OTHER INFORMATION

(Including Author, Title, Date, Pertinent Pages, Etc.)

*Examiner Cite
Initial No.
None

Examiner

Date Considered

Michael Tril

5/5/2005

*Examiner: Initial if reference considered, whether or not citation is in conformance with M.P.E.P. § 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

JEN:hjd

F1 = Only English Abstract

LAW OFFICES OF
CHRISTENSEN O'CONNOR JOHNSON KINDNESSTM
1420 Fifth Avenue
Suite 2800
Seattle, Washington 98101
206.682.8100